WHAT IS CLAIMED IS:

1. A semiconductor processing component comprising SiC, wherein an outer surface portion of the component has a surface impurity level that is not greater than 10 times a bulk impurity level.

2. The component of claim 1, wherein the bulk impurity level is measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

3. The component of claim 1, wherein the outer surface portion is comprised of CVD-SiC.

4. The component of claim 3, wherein the outer surface portion is a CVD-SiC layer deposited over a substrate.

5. The component of claim 4, wherein the substrate comprises SiC.

6. The component of claim 5, wherein the substrate comprises SiC impregnated with elemental silicon.

7. The component of claim 6, wherein the substrate comprises recrystallized SiC impregnated with elemental silicon.

8. The component of claim 4, wherein the CVD-SiC layer has a thickness within a range of about 10 to about 1000 μm.

9. The component of claim 4, wherein the CVD-SiC layer has a thickness within a range of about 10 to about 800 μm.

10. The component of claim 3, wherein the component is a free-standing CVD-SiC component.

11. The component of claim 10, wherein the component consists essentially of CVD-SiC.

12. The component of claim 1, wherein the surface impurity level is not greater than 5 times the bulk impurity level.

13. The component of claim 1, wherein the surface impurity level is not greater than 2 times the bulk impurity level.

14. The component of claim 1, wherein the surface impurity level is not greater than the bulk impurity level.

15. The component of claim 1, wherein the surface impurity and bulk impurity levels are based on at least one of Cr, Fe, Cu, Ni Al, Ca, Na, Zn, and Ti concentrations

16. The component of claim 15, wherein the surface impurity and bulk impurity levels are based on at least one of Cr and Fe concentrations.

17. The component of claim 16, wherein the surface impurity and bulk impurity levels are based on Fe concentration.

18. The component of claim 16, wherein the bulk impurity level is not greater than 1E17 atoms/cc Fe and not greater than 1E15 atoms/cc Cr.

19. The component of claim 1, wherein the semiconductor processing component comprises a component from the group consisting of semiconductor wafer paddles, process tubes, wafer boats, liners, pedestals, long boats, cantilever rods, wafer carriers, process chambers, dummy wafers, wafer susceptors, focus rings, suspension rings.

20. The component of claim 19, wherein the component is a wafer boat.

21. The component of claim 1, wherein the component is machined prior to treatment to provide said surface impurity level.

22. A method for treating a semiconductor processing component, comprising:

providing a semiconductor processing component having an outer surface portion formed by chemical vapor deposition of SiC, the outer surface portion having a bulk impurity level and a surface impurity level; and

removing a target portion of the outer surface portion, such that the surface impurity level is not greater than 10 times the bulk impurity level.

23. The method of claim 22, wherein the surface impurity level is not greater than 5 times the bulk impurity level.

24. The method of claim 22, wherein the surface impurity level is not greater than 2 times the bulk impurity level.

25. The method of claim 22, wherein the surface impurity level is not greater than the bulk impurity level.

26. The method of claim 22, wherein the target portion is removed by reacting the target portion.

27. The method of claim 26, wherein reacting is oxidizing such that the outer surface portion forms an oxide, and the step of removing the target portion further includes removal of the oxide.

28. The method of claim 27, wherein oxidizing and removal of the oxide are repeated to remove said target portion.

29. The method of claim 27, wherein the step of oxidizing is carried out at a temperature within a range of about 950 to about 1300 degrees C.

30. The method of claim 27, wherein the step of oxidizing is carried out in a wet ambient atmosphere.

31. The method of claim 26, wherein the target portion is removed by etching.

32. The method of claim 31, wherein etching includes reacting the target portion with an etchant species to form an etchant product, the etchant product volatilizing to remove the target portion.

33. The method of claim 32, wherein the etchant species is a Cl-containing gas, forming a $SiCl_x$ etchant product.

34. The method of claim 22, further comprising reacting contaminants present at an outer surface of the outer surface portion to form a reaction product.

35. The method of claim 34, wherein the target portion is removed by oxidizing the outer surface portion to form an oxide followed by removal of the oxide, and the steps of reacting and oxidizing are carried out simultaneously.

36. The method of claim 34, wherein the reaction product volatilizes after formation, improving purity of the component.

37. The method of claim 34, wherein the reaction product has a higher volatility than the contaminant.

38. The method of claim 34, wherein the contaminants are reacted with a halogen gas.

39. The method of claim 34, wherein the halogen gas comprises a halogen from the group consisting of chlorine and fluorine.

40. The method of claim 39, wherein the halogen gas comprises HCl.

41. The method of claim 38, wherein the halogen gas is present at a partial pressure within a range of about 0.01 to about 10%.

42. The method of claim 22, wherein the semiconductor processing component comprises a component from the group consisting of semiconductor wafer paddles, process tubes, wafer boats, liners, pedestals, long boats, cantilever rods, wafer carriers, process chambers, dummy wafers, wafer susceptors, focus rings, suspension rings.

43. The method of claim 22, wherein the semiconductor processing component comprises a substrate, the outer surface portion being a coating overlying the substrate.

44. The method of claim 43, wherein the substrate comprises elemental silicon.

45. The method of claim 44, wherein the substrate comprises silicon carbide with said elemental silicon impregnated thereon.

46. The method of claim 22, wherein the target portion is removed prior to use in a semiconductor processing operation.

47. The method of claim 22, wherein target portion is removed by repeating removal steps.

48. The method of claim 22, wherein the target portion has a thickness of at least 0.25 μm.

49. The method of claim 22, wherein the target portion has a thickness of at least 0.38 μm.

50. The method of claim 22, wherein the target portion has a thickness of at least 0.50 μm.

51. The method of claim 22, further comprising machining the component prior to removing of the target portion.

52. A method for treating a semiconductor processing component, comprising:

providing a semiconductor processing component having an outer surface portion formed by chemical vapor deposition of SiC, the outer surface portion having a bulk impurity level and a surface impurity level; and

removing a target portion of the outer surface portion, such that the surface impurity level is reduced at least 10x.

53. The method of claim 52, wherein the surface impurity level is reduced at least 100x.